DRAM

LPDDR2 DRAM

Features:

- Low-voltage Core and I/O Power Supplies
  VDD2 = 1.14-1.30V
  VDDCA/VDDQ = 1.14-1.30V
  VDD1 = 1.70-1.95V
- High Speed Un-terminated Logic
  (HSUL_12) I/O Interface
- Clock Frequency Range :
  10MHz to 533MHz
  (data rate range : 20Mbps to 1066 Mbps per I/O)
- Four-bit Pre-fetch DDR Architecture
- Multiplexed, double data rate, command/address inputs
- 4 or 8 internal banks for concurrent operation
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable Read/Write latencies (RL/WL) and burst lengths (4,8 or 16)
- Per-bank refresh for concurrent operation
- ZQ Calibration
- On-chip temperature sensor to control self refresh rate
- Partial –array self refresh (PASR)
- Bank & Segment masking
- Deep power-down mode (DPD)

Options:

- x16
- x32

Package:

- 134-ball BGA
- 168-ball PoP BGA

Densities:

- 2Gb
- 1Gb
- 512Mb
- 256Mb

Clock Frequencies:

- 533 MHz
- 400 MHz
- 333 MHz

Temperature Grades:

- Commercial (0°C to 85°C)
- Industrial (-40°C to 85°C)
- Automotive, A1 (-40°C to 85°C)
- Automotive, A2 (-40°C to 105°C)
- Automotive, A25 (-40°C to 115°C)