

Advancements In Packaging Technology Driven By Global Market Return

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Recently, the focus of attention in the IC packaging industry has been squarely on removing costs from the manufacturing supply chain. As the economic recovery accelerates, however, advances in innovative IC package design and manufacture are likely to lead the headlines. IC integration technologies, in particular, such as wafer-level packaging design, through silicon via (TSV) technology – especially in the area of IC/memory integration – and an explosion of new developments in the area of multi-die and die stacking technologies are poised to move the industry further and faster than in recent years. This paper will review how materials suppliers have invested significant resources to deliver market-ready materials aligned with this renewed emphasis on packaging technology development.

An Industry in Recovery

Recent statistics regarding inventory levels and corporate earnings suggest that the semiconductor packaging market appears to be recovering from the Q4 2008 – Q1 2009 low point much faster than many industry experts had anticipated. Sales and unit volume shipments of NAND flash between January and July of 2009 increased by 98% and 67% respectively, with similar increases realized for DRAM, analog and microprocessors (1). Industry analysts are now projecting the market for ICs to show strong growth through 2010 and 2011, with even a potential for industry-wide wafer fab utilization being maxed out in the coming months, resulting in longer lead times, spot shortages and escalating average selling prices throughout the industry (2).

Though the improvements seem to be occurring in a wide range of markets and applications, recovery in some segments is following a faster curve than others. Over proportional growth in emerging markets coupled with new applications in advanced packaging is driving packaging engineers to exploit recent advances in packaging technology. IC integration technologies, for example, including new wafer-level packaging design, through silicon via (TSV) technology – especially in the area of IC/memory integration – and an explosion of new developments in the area of multi-die and die stacking technologies are poised to move the industry further and faster than ever before in high density die packaging. Halogen-free initiatives are driving the redesign of entire families of products. And, finally, the rapid growth of new photovoltaic, automotive and display technologies are advancing the development of new IC package designs.

Materials suppliers have invested significant resources to deliver market-ready materials aligned with this renewed emphasis on packaging technology development. Examples which will be reviewed in this paper include:

- Wafer backside coating materials developed for thinner bondlines, lower total package cost and improved manufacturing throughput.
- Innovations in compression molding technology for wafer-level redistribution applications.
- Passive and active materials for the robust, low-cost production of photovoltaic devices, which are helping to define an entire new market segment.
- Thermo-compression bonding materials for low-cost flip-chip manufacturing.
- Epoxy-flux materials for improved CSP package assembly yield and reliability

These technologies, among others, will accelerate a strong recovery in the IC packaging market in 2010.

Packaging Materials Innovations

Throughout the recent global economic downturn, companies with an eye to the future have continued (or accelerated) investments in research and development. The IC packaging and design industry is no exception. As the economic recovery gathers speed, advances in innovative IC package design and manufacture are likely to lead the headlines. The following innovations highlight this movement:

Wafer Backside Coating for Leadframe/Power IC Packages

Traditional silver-filled die attach adhesives have been successfully employed to bond ICs to leadframes and laminate substrates for decades. In a conventional die attach process, paste is dispensed onto the leadframe pad and the chip placed into the paste. The leadframe pad must be designed significantly larger than the chip, to allow for the flow of the paste and the formation of a fillet around the die edge. In addition, the die must have a minimum thickness to prevent the paste flowing onto the top surface of the chip. To address these issues, Wafer Backside Coating (WBC) technology has been developed. WBC is a b-stage paste that is coated on the backside of a wafer prior to dicing (Figure 1). WBC provides fillet control for reduced package size, bondline thickness (BLT) control for reduced die tilt and minimal processing steps for reduced manufacturing cost.

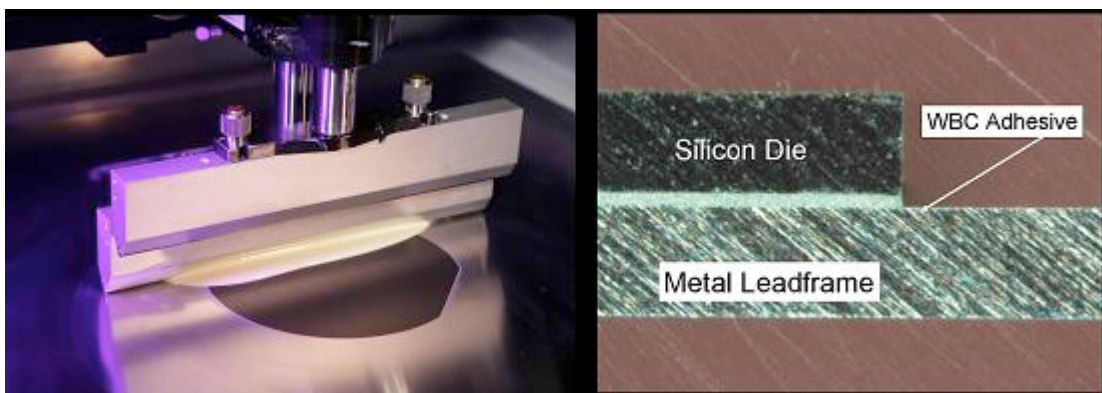


Figure 1. WBC application onto wafer prior to dicing and after die placement

In test packages assembled using the WBC technology, a consistent 25-micron print thickness was achieved over a period of several hours of continuous printing.

Additionally, optimal die assembly parameters were established using a 4mm x 4mm die size, 10N bondforce, 1000msecs bond time, and 130°C die attach temperature. Finally, functional packages were assembled using the WBC technology and subjected to MSL Level 1 / 260°C reliability testing. Using two die sizes (0.5x0.5mm and 1.5x1.5mm) on NiPdAu leadframes, all packages passed MSL Level 1 / 260°C.

Compression Mold Materials

Compression molding is gaining ground as an alternative to transfer molding in various applications including eWLB, MCP, SiP and others. The benefit in utilizing compression molding is that a larger area can be molded at once, improving manufacturing throughput, while also minimizing waste. Additionally, compression molding eliminates various materials and/or process steps used in advanced packages, such as the elimination of laminate substrates in some WLSCP packages and the elimination of underfill processes in FC-CSP packages.

As an example, eWLB (embedded wafer level package), a WL-CSP, is made in a batch process starting from a “virtual wafer”. This next generation wafer level package uses a fan-out design, which enables higher I/O and the use of known good die (KGD) – both factors helping to reduce overall package cost. Compression molding technology is being used for this application to realize a previously unachievable target of 0.5mm warpage across an 8-inch wafer area. The compression molding material possesses unique process and performance that enable this package design. Both liquid and powder compression molding materials are being developed for this application.

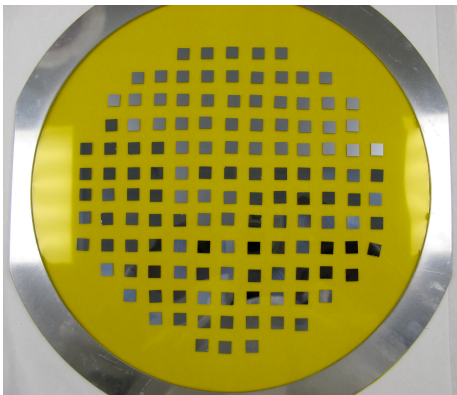


Figure 2. eWLB-type package before and after compression molding

Electrically Conductive Adhesives for Assembly of Photovoltaic Modules

Next generation flexible thin film, dye sensitized and/or organic solar cells often rely on temperature sensitive substrates. Making an electrical interconnection onto these flexible substrates requires low temperature interconnection processes, eliminating traditional SnPb and lead-free SnAgCu soldering processes from consideration. Electrically conductive adhesives have been used for many years as an alternative to traditional solders in high reliability electronics applications such as satellite, automotive, medical and telecommunication electronics. The major limitation of electrically conductive adhesives, however, has been their instability on non-noble electronic termination metals such as copper and Sn.

To address this limitation, new innovations in conductive adhesives have been achieved. Recent work has shown that the unstable contact resistance of electrically conductive adhesives on copper and tin is due to electrochemical corrosion of these metals under elevated temperature and humidity conditions. (3) Based on the above fundamental understandings, a new class of conductive adhesives has been developed which exhibit exceptional contact resistance stability on surfaces including OSP copper, Sn alloys and even 100% Sn. The result is a new electrically conductive adhesive product line for use on thin film solar substrates.

To demonstrate the performance of these new electrically conductive adhesives for thin-film solar cell applications, a test device having indium tin oxide (ITO) terminations was bonded to non-noble metal interconnection tabs using the electrically conductive adhesives. Contact resistance measurements were performed according the TLM-method, as described by Herz et al. (4). The results of this testing are illustrated in Figure 3, in which the new conductive adhesives designed for compatibility with non-noble interconnects (samples A, E, F) exhibit stable electrical contact between ITO and a Sn termination through 1000-hours of 85°C/85%RH exposure..

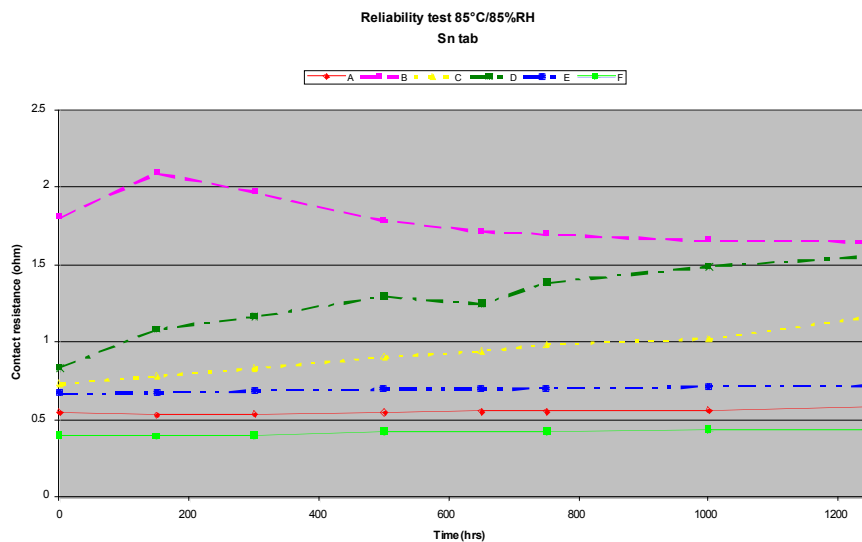


Figure 3. Contact resistance stability under 85%RH/85°C conditions of conductive adhesives when bonding a Sn metallized tab onto ITO-coated glass

As the electrically conductive adhesives are processed at temperatures significantly below the melting temperature of traditional SnPb and lead free SnAg solders, the reliability data from this report, indicate that electrically conductive adhesives containing new corrosion inhibitors are a viable alternative to solder interconnections for applications requiring low-temperature processing.

Thermo-compression Flip-Chip

In addition to their use in microprocessors, flip-chip packages are now also being used in many IC packages. Typically these flip-chip devices use solder reflow to form the electrical interconnect. However, for very fine-pitch devices, conventional solder reflow cannot be used due to solder bridging. Recent work (5) has shown that thermo-compression bonding (TCB) may be used for a growing number of very fine-pitch flip-

chip applications, including copper pillar and gold stud flip-chip interconnects, when aided by a new NCP underfill material.

The new non-conductive paste (NCP), offering fast bonding time and good reliability performance, has been designed for copper pillar and Au stud-bump flip-chip interconnect processing. Analysis has shown that flip-chip bonding using this new NCP can occur in as little as one-second bond time (Figure 4).

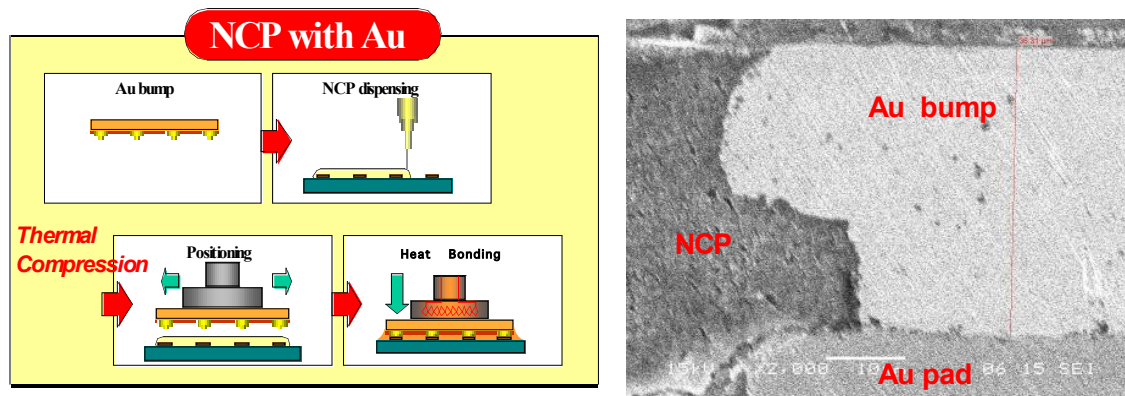


Figure 4. Thermo-compression flip-chip process and cross-section

Thermo-compression flip-chip devices were assembled using the new NCP material. After bonding, the devices were subjected to MSL L3/260°C and HAST testing. For all tests, 100% yield and passing MSL/HAST performance was reported at most bonding conditions.

Epoxy Flux Technology for Improved Reliability Solder Interconnections

Since their inception over 30 years ago, underfill materials have enabled numerous new package designs by providing mechanical support and reliability for miniaturized solder interconnections. But, as the industry continues its march forward toward higher density, flexible and miniaturized devices and component configurations, traditional underfill materials fail to meet the needed demands. A breakthrough underfill material technology called epoxy flux has recently been developed. Designed to offer process efficiency, epoxy flux underfills deliver a fluxing component that facilitates solder joint formation as well as an epoxy system that offers added device protection by encapsulating individual bumps (Figure 5). Because epoxy fluxes are cured during the reflow process, they offer an in-line alternative to other underfill methods and, depending on the process, may eliminate the need for a dedicated dispensing system and the time required to dispense and cure. These new materials also provide deposition flexibility and, depending on the application and process, can be screen printed, dipped, jetted or dispensed as required.



Figure 5. CSP device assembled using epoxy-flux technology (after reliability testing)

In a recent analysis of PoP attachment reliability, several fluxing materials were studied: No-clean tacky fluxes, SAC 305 solder paste and epoxy flux. The devices were subjected to drop testing (JEDEC 22-B111, horizontal dropping, 2900G, 0.3msec, 10% resistance criteria), and results indicate that epoxy flux offers the most robust performance with the most number of drops before the first failure as well as the longest characteristic life (Table 1).

TABLE I. Drop-Shock Test Results

Interconnect Process	1 st Failure (# of drops)	Characteristic Life (# of drops)
Solderpaste (Type IV)	1	3.5
Epoxy-Flux (2.5-mil dip)	4	32
Epoxy-Flux (6-mil dip)	10	98

Epoxy flux material technology provides improved manufacturing rates through enhanced throughput and improved reliability required for fine-pitch assembly. With a dual function flux and underfill in one material, epoxy fluxes have a broad application range for both packaging and board assembly environments. In addition to CSP array package attach and reinforcement, these new materials are finding application in ball attach processes for BGA and CSP performance improvement.

Conclusions

As the economic recovery accelerates in 2010, advances in innovative IC package design and manufacture are likely to lead the headlines. As in previous recessionary periods, those companies that continued to invest in new technologies and manufacturing efficiencies during the recent market downturn will be the first to come to market with technology-leading new products (6). Several novel packaging materials technologies, such as WBC, NCP flip-chip bonding, non-noble conductive adhesive bonding and compression molding materials are likely to lead the way towards new innovative package designs.

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