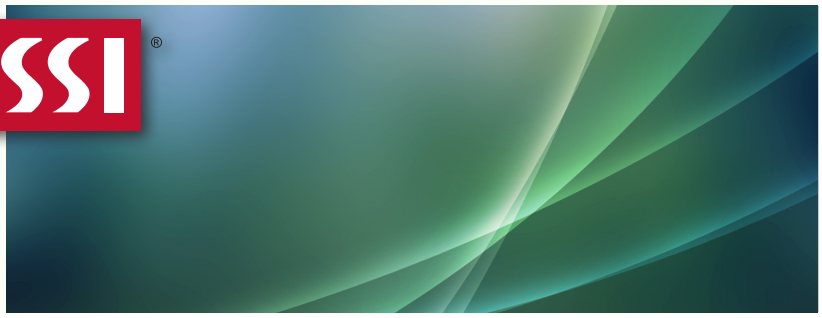

DRAM

Mobile DDR SDRAM

Ideal for applications requiring memory bandwidth and low-power

▶ Features:

- Standard double-data rate clock timing
- Four internal banks with bank controls
- Data masking per byte on Write commands
- Programmable burst length of 2, 4, or 8
- Programmable CAS Latency of 2 or 3
- Auto-Refresh and Self-Refresh Modes
- Auto-Precharge Supported
- JEDEC compliant BGA: 60-ball (x16)
- 90-ball (x32), 152-ball PoP BGA (x32)

▶ Clock Frequency:

- Low supply voltage: 1.8V +/- 0.1V
- Clock Stop, Power Down, and Deep Power Down Modes (DPD)
- Extended Mode Register (EMR)
  On-chip Temperature Compensated Self-Refresh (TCSR)
  Partial Array Self-Refresh (PASR)
  Selectable Output Drive Strength (DS)

Density	Configuration	Part Number
32Mb	2M x 16	IS43LR16200D
	1M x 32	IS43LR32100D
64Mb	4M x 16	IS43LR16400C
	2M x 32	IS43LR32200C
128Mb	8M x 16	IS43LR16800G
	4M x 32	IS43LR32400G
256Mb	16M x 16	IS43LR16160G
	8M x 32	IS43LR32800G
512Mb	32M x 16	IS43LR16320C
	16M x 32	IS43LR32160C
1Gb	64M x 16	IS43LR16640A
	32M x 32	IS43LR32320B
2Gb	64M x 32	IS43LR32640A

Notes:
1. Automotive grade mDDR part numbers begin with “IS46LR”.
2. Please check for availability of PoP BGA package options.

Options

Clock cycle time	
6ns (166MHz)	-5
5ns (200MHz)	-6
Package	
Leadfree BGA	BL
Leadfree PoP BGA	BPL
Temperature grades	
Commercial (0°C to +70°C)	(blank)
Industrial (-40°C to +85°C)	I
Automotive A1 (-40°C to +85°C)	A1
Automotive A2 (-40°C to +105°C)	A2
Automotive A25 (-40°C to +115°C)	A25

512Mbit Power Specification

Operating Burst Read	IDD4R	100mA max.
Precharge Power Down Standby	IDD2PS	300mA max.
Full Array Self-Refresh	IDD6	700µA max.
Deep Power Down	IDD8	10µA max.